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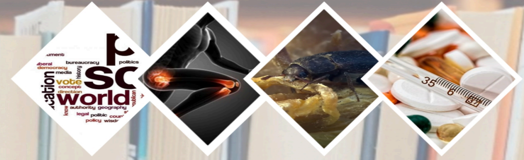

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C-V and G-V Studies Formed by Low Energy Dual Ion Implantation

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Abstract

Silicon oxynitride ($Si_xO_yN_z$) thin insulating films were synthesized by sequential implantation of reactive ion-beams of $^{16}O_2^+$ and $^{14}N_2^+$ in the ratio 1:1 into silicon at room temperature to total fluence level of 1.0×10^{18} cm^{-2} at 30 keV energy. The high frequency capacitance-voltage (C-V) and conductance-voltage (G-V) studies performed at room temperature on MIS devices fabricated with as implanted as well as rapid thermal annealed (RTA) samples reveal the presence of interface traps. The interface state density distribution showed U- shaped features with midgap value ~$1.61\text{-}1.81\times10^{10}$ eV^{-1} cm^2 discrete peaks in the lower as well as higher energy range after annealing. The G-V studies show that there is less contribution from series and bulk states. The conductance is found to be increasing with increase in annealing temperature.

Keywords: Silicon oxynitride, C-V, G-V, RTA

1. Introduction

Silicon oxynitride thin film has large potential applications in various integrated optical devices because of its excellent optical properties and low absorption losses in near infrared wavelength range [1]. As it incorporates positive features of both SiO_2 and Si_3N_4, it gives a large degree of freedom for the design of integrated optics [2]. In these paper silicon oxynitride ($Si_xO_yN_z$) thin insulating films were synthesized by sequential implantation of reactive ion-beams of $^{16}O_2^+$ and $^{14}N_2^+$ in the ratio 1:1 into silicon at room temperature to total fluence level of 1.0×10^{18} cm^{-2} at 30 keV energy. The electrical characterizations of ion-beam synthesized silicon oxynitride have been carried out using the high and low frequency capacitance-voltage (C-V) and conductance-voltage (G-V) studies at room temperature on MIS devices fabricated with as implanted as well as rapid thermal annealed (RTA) samples.

2. Methodology

Single crystal silicon wafers (p-type, 0.8-1.2 Ω-cm resistivity and <111> orientation) were used as substrate material. The silicon wafers were thoroughly cleaned adopting standard RCA-I and RCA-II cleaning procedures using electronic grade chemicals and distilled deionized (DI) water. These wafers were then cut into sizes of 1cm × 1cm samples for loading onto the sample holder of the implanter. To synthesize the silicon oxynitride insulating layers, samples were implanted with $^{16}O_2^+$ and $^{14}N_2^+$ in the ratio 1:1 into silicon at room temperature to total fluence level of 1.0×10^{18} cm^{-2} at 30 keV energy. The samples with oxygen to nitrogen ratio of 1:1 were prepared using the 30 keV ion-implantation facility available in the Department of Physics, Mumbai University in a vacuum of ~1.0×10^{-5} mbar. For uniform implantation over 1 cm^2 area and to reduce the ion-beam heating effects, magnetic field scanning of the ion beam was employed. Dry O_2 and N_2 high-purity gases were used as the ion source feed-in material. Ion-beam current density of 3–8 μA cm^{-2} was used for implantation. For electrical measurement high purity (99.999%) aluminum metal film was deposited on to the unimplanted unpolished side of the sample in a vacuum of the order of 5.0×10^{-7} mbar. During deposition, the sample was placed on a clean stainless steel substrate heater in the evaporation system heated at a temperature of 450 °C and maintained for 45 minutes in vacuum of 1.0×10^{-7} mbar. Aluminium contacts dots of diameter 0.75mm were evaporated through mechanical masks onto the top of the insulating layers to complete the MIS structures. The C-V and G-V measurements were performed on a Hewlett Packard Precision LCR meter, model HP 4284A.

3. Results and Discussion

Capacitance-Voltage (C-V) Studies

Fig. 1. shows the C-V characteristics of MIS structures with ion beam synthesized silicon oxynitride ($Si_xO_yN_z$) layers (un-annealed and post implantation RTA at 673 K, 873 K and 1173 K for 5 min). The high frequency (1 MHz) C-V characteristics of unannealed Al-$Si_xO_yN_z$-Si (MIS) devices fabricated with the silicon sample implanted at a fluence of 1.0×10^{18} cm^{-2} do not show any significant variation of capacitance with applied voltage. This shows that silicon below the ion beam synthesized silicon oxynitride ($Si_xO_yN_z$) is highly damaged. The C-V characteristics of ion beam synthesized silicon oxynitride ($Si_xO_yN_z$) layers after RTA at

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673 K and 873 K for 5 min shows some variation in capacitance with applied voltage indicating slight recovery of the damaged silicon layer to monocrystalline. Further increase in the annealing temperature at 1173 K exhibiting a strong field dependence characteristic of MIS structures such as the accumulation, depletion and inversion regions are clearly distinguished in the C-V curve. The C-V curve indicates that after rapid thermal annealing at 1173 K for 5 min, the electrically dead layer of the damaged silicon has recovered to monocrystalline from, thus giving rise to good silicon – insulator interface. The thickness of the ion beam synthesized oxynitride layer calculated from C-V measurements is shown in table 1.

Table 1: Capacitance of silicon oxynitride, thickness of silicon oxynitride layer and thickness of damaged silicon beneath the ion-beam synthesized $Si_xO_yN_z$ MIS structures at different temperatures after annealing

Sr. No.	Annealing Condition	C_i (pF)	d_i (nm)	d_{asi} (nm)
1	Room Temp.	13.82	1611.5	3193.8
2	673 K	50.19	443.7	756.0
3	873 K	110.20	202.0	251.7
4	1173 K	271.5	82.0	1.1

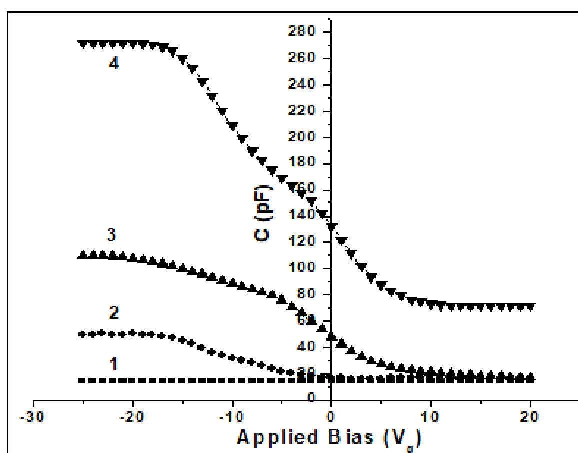

Fig 1: High frequency C-V characteristics of as-implanted $Al/Si_xO_yN_z/Si$ structure synthesized at fluence of 1.0×10^{18} cm^{-2} and O: N ratio of 1:1: (1) unannealed; (2) annealed at 673 K; (3) annealed at 873 K; (4) annealed at 1173 K for 5 min.

The midgap value of the interface state density is ~ 1.18×10^{10} eV^{-1} cm^2. The interface state density at the midgap in the present work after annealing the ion beam synthesized oxynitride is of the same order as observed by other authors for oxynitride films synthesized by other methods.

Conductance-Voltage (G-V) Studies

The G-V characteristics of MIS structures with ion beam synthesized silicon oxynitride ($Si_xO_yN_z$) layers (un-annealed and post implantation RTA at 673 K, 873 K and 1173 K for 5 min) as a dielectric are represented in Fig. 2. The conductance increases with increasing annealing temperature and the peak becomes broader. The position of the peak moves towards zero gate voltage with increasing annealing temperature. This indicates that the traps are distributed almost uniformly inside the silicon gap. As the applied bias is increased the energy is moved towards the Fermi level and thus into an area of less interface traps. The conductance is observed due to interface states present in the silicon and only series and bulk states can contribute to this conductance. The G-V characteristics of MIS capacitors annealed at 1173 K observed at different frequencies shows the conductance increases with increasing measurement frequency. The observed conductance peaks are smaller indicating reduction in interface defect concentrations as expected contribution from the annealing.

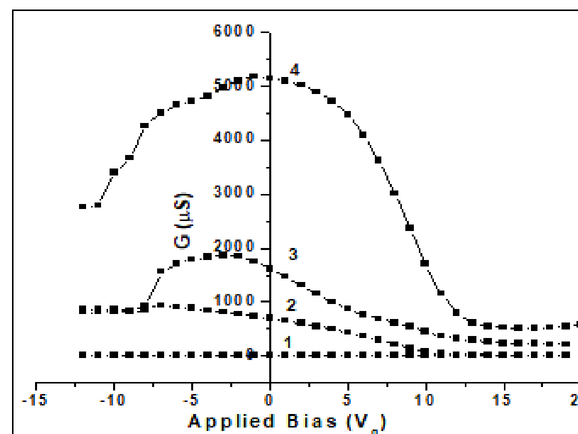

Fig 2: G-V characteristics of $Al/Si_xO_yN_z/Si$ structure synthesized at fluence of 1.0×10^{18} cm^{-2} and O: N ratio of 1:1: (1) unannealed; (2) annealed at 673 K; (3) annealed at 873 K; (4) annealed at 1173 K for 5 min.

4. Conclusion

Silicon oxynitride ($Si_xO_yN_z$) thin insulating films were synthesized by sequential implantation of reactive ion-beams of $^{16}O_2^+$ and $^{14}N_2^+$ in the ratio 1:1 into silicon at room temperature to total fluence level of 1.0×10^{18} cm^{-2} at 30 keV energy. The high frequency capacitance-voltage (C-V) and conductance-voltage (G-V) studies performed at room temperature on MIS devices fabricated with as implanted as well as rapid thermal annealed (RTA) samples reveal the presence of interface traps. The interface state density distribution showed U- shaped features with midgap value ~$1.61\text{-}1.81\times10^{10}$ eV^{-1} cm^2 and discrete peaks in the lower as well as higher energy range after annealing. The G-V studies show that there is less contribution from series and bulk states. The conductance is found to be increasing with increase in annealing temperature.

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